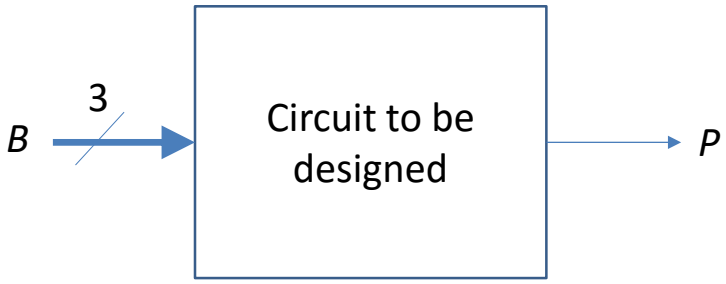
Digital Electronics

The purpose of this exercise is to synthesize a parity check circuit. The output should be activated at '1' if the datum *B* contains an odd number of '1' and it should be '0' if *B* has an even number of '1'.



P=1 if *B* has an odd number of 1
P=0 otherwise (*B* has an even number of 1)

1.1 Draw the truth table of *P* signal in a 3-input Karnaugh map. Justify that the canonic SOP (sum-of-products) expression cannot be simplified by the Karnaugh simplifying technique.

1.2 Give the SOP expression of *P*. Simplify it by factorizing the expression.

1.3 Propose and justify a diagram that assembles one-input or 2-input logic gates (NOT, AND, OR, NAND, NOR, XOR). The number of gates should be minimized.

1.4 For each gate used in the question above, give its CMOS diagram (assembling NMOS and PMOS transistors).

1.5 Propose another CMOS circuit by directly synthesizing the combinational function *P* by using the 'constant transmission' technique.

1.6 Compare the number of transistors in both circuits. Which one occupies the smallest area?